HDL DESIGN FOR ULTRA HIGH MULTI FREQUENCY CLOCK RATE-MULTI CHANNEL PRBS UNIVERSAL DATA SCRAMBLER DESCRAMBLER ASIC IP CORE

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ABSTRACT: Scrambler De-Scrambler is a device used to encode and decode the message data in to randomized(Seed words) data.. This paper deals Design of High Speed Multichannel Universal Data Scrambler De-ScramblerOf Different Data Rates (Giga/Tera Bit Rate) for Ultra High Speed Wireless Applications like Gigabit WIMAX,WIFI,3G,4G,Parallel Data Computing, Internet, Cloud Computing etc. Scrambling Different PRBS Data as perCCITT – ITU Standards. This Design consists of Different Pattern Sequence based PRBS Generators & XOR Gates for encryption and decryption of digital data either serially/parallel. Design using Xilinx ISE 9.2i Software,Programming done by using VHDL & Verilog HDL, Design Implementation on Latest Xilinx Spartan III FPGA Kit.

KEYWORDS: Gbps – Giga Bits Per Second, Tbps- Tera Bits Per Second, Wi-Fi- Wireless Fidelity , PRBS- PseudoRandom Binary Sequence, CCITT- Consulting Committee for International Telegraph and Telephone, FPGA-FieldProgrammable Gate Array, ISE- Integrated Software Environment, VHDL– Very High Speed Integrated CircuitHardware Description Language.

INTRODUCTION

In Modern Digital Communication Systems and Applications, Products, Scrambler-Descrambler very important component for encryption and decryption of randomized digital data In the form seed words in cipher text format Basically this universal data scrambler designed by using Linear Feed Back Shift Register and XOR gates. The length of Universal Scrambler is 2^n-1. Scrambling done at the transmitter side for encryption of digital data and descrambling done at the receiver side for decryption of Randomized Digital Data. For Implementation of Different Communication Protocols , Scrambling and Descrambling Reduce the Noise in the Data Codes, Error Rate of Transmission and Reception. Scrambler – Descrambler IP Cores are Very Suit for HiFi-Hitech Smart Computing wireless Communication Products likeWi-Fi,Gi-Fi, WCDMA,CDMA, 3G,4G Wireless Communication Products , Wireless Network On Chip Transceivers, Wireless Network Routers, GPS,GSM,GPRS, Bus Communication Network Protocols. Wi-Max.Transceivers,OFDMA Transceivers.

Notations:
D = Delay element,S = Scrambler Input,D^xS = A sequence S delayed by x bits,m, n = Length of registers,T1 = Scrambler Output,T2 = Descrambler Input,R1,R2 = Registers

Multi Clock Frequency Generator / Oscillator

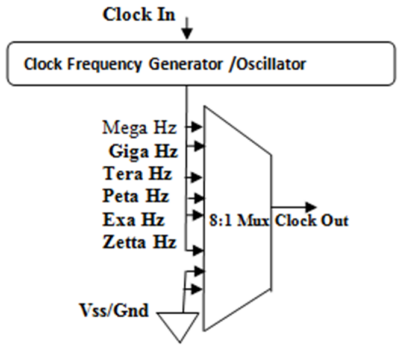

Figure 1.Ultra High Multi Clock Frequency Generator

Description—Multi Clock Frequency Generator consists Clock Frequency Generator/Oscillator, 8:1 Multiplexer. Clock Frequency Generator . Generator consists Counter to Generates Different Clock Frequencies, MHz,GHz,THz,PHz,EHz,ZHz of 10^6 or 2^{20}, 10^9 or 2^{30}, 10^{12} or 2^{40}, 10^{15} or 2^{50} ,10^{18}or 2^{60} ,10^{21}or 2^{70} Clock Cycles. 8:1 Multiplexer Selects The one the above frequencies to generate Baud Rate of Specific Clock. Frequencies to Scrambler /Descrambler ASIC IP Core for High Speed Wireless Data Security Products.

Scrambler ASIC IP Core/Generator

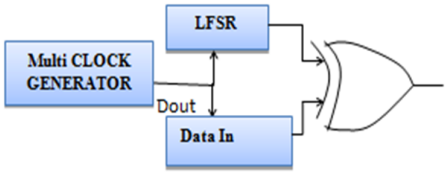

Figure 2. Scrambler Block Diagram

Description— Scrambler Design Consists Multi Clock Frequency Generator and LFSR-Linear Feed back Shift Register, Data Register and Data input is in XOR with LFSR Feedback output Generates Scrambler Output for Wireless Data Security Products/ Applications.

Sequence of LFSR and Data Values for Scrambler

Description—Data Values/Bits in the Data Register and LFSR Random sequence Patterns (Seed Words) are XOR'ed and generates Scrambler Design output for Encrypting the Data of Plain Text to Cipher Text Format.

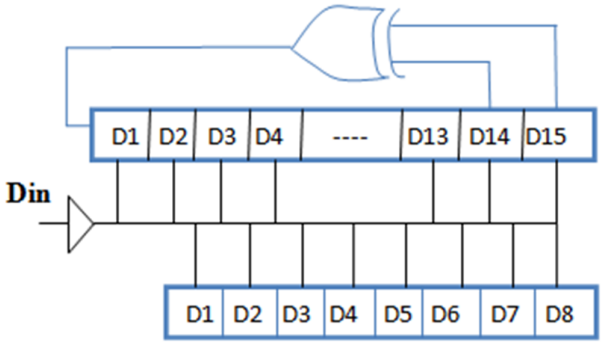

Figure 3. Sequence Of LFSR and Data in Values in the Scrambler

Encryption/Decryption

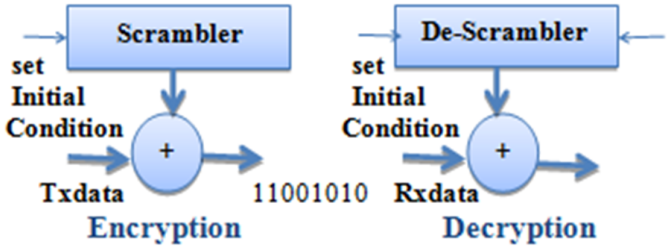

Figure 4. Data Encryption Decryption using Scrambling Descrambling

Description—Data encryption Encoding and Data Decryption Decoding Done by Scrambler and De-Scrambler IP Core Generator.

HIGH SPEED MULTICHANNEL SCRAMBLER DE-SCRAMBLER DESIGN ARCHITECTURE AS PER ITU STANDARDS

Description

The Design Architecture Consists of Data Selector / De-selector (Mux/De-Mux) for selecting and Deselecting Different Scrambled Descrambled PRBS Data Sequence Patterns (Seed Words) of Different Data Rates as per CCITT ITU Standards. Scrambled / De-Scrambled Data Sequences PRBS-7, 10,15,23,31 pattern sequences XORed with Data Register Pattern. The Data Selector is used synchronize different randomized data sequence frames. Data Selector selects different Scrambled Data Sequences of Different PRBS Pattern sequences 7, 10,15,23,31 by XORed with Data Register and send the scrambled data serially through serialized link. De-serialize the data sequence frames by using De-multiplexer as a De-selector to distribute the Descrambled data to original message data by Decrypting.

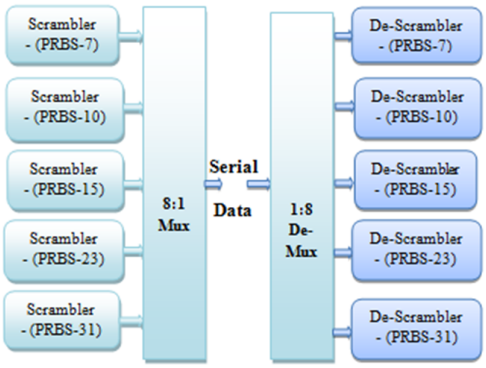

Figure 5. High Speed Multi Channel Scrambler-De-Scrambler Design Architecture

SIMULATION WAVE FORM REPORTS

Simulation-Scrambler ASIC IP Core

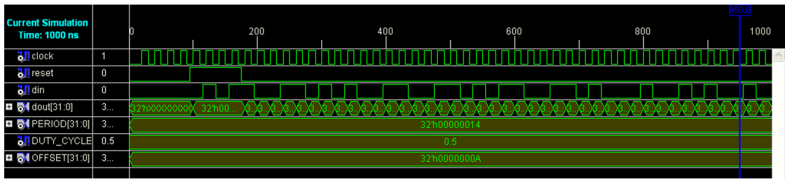

Figure 6. Scrambler IP Core

MultiChannel Scrambler IP Core

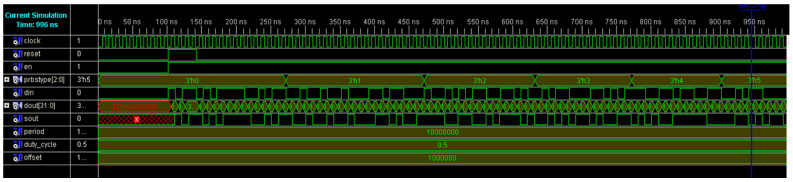

Figure 7. Multichannel Scrambler IP Core

Serial Scrambler IP Core

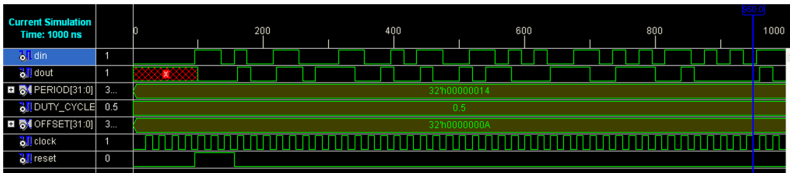

Figure 8. Serial Scrambler ASIC

DESIGN FLOW REPORTS

RTL Design Block Scrambler ASIC IP

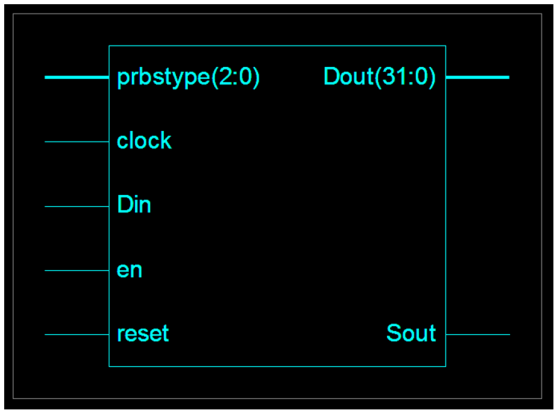

Figure 9. Scrambler ASIC

RTL Schematic Scrambler ASIC IP Core

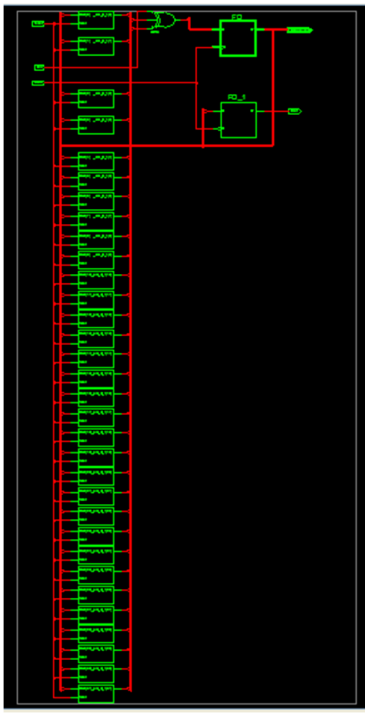

Figure 10. Schematic Of Scrambler ASIC

FPGA Placed Design Report
Scrambler ASIC IP Core

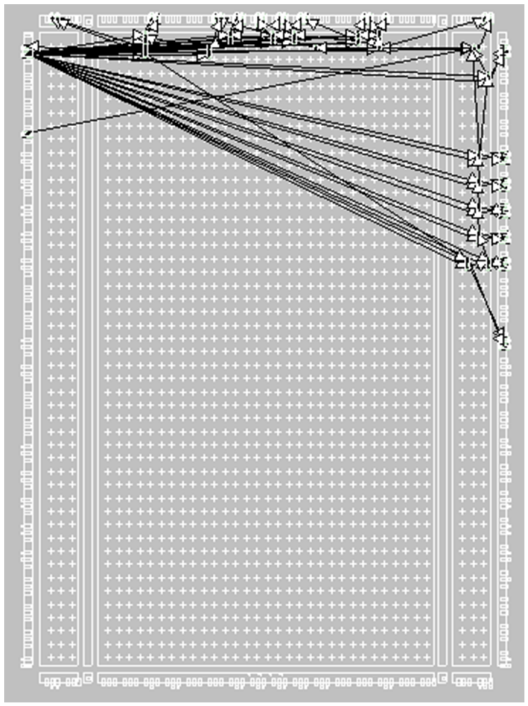

Figure 11. Scrambler ASIC Placed Design Report

FPGA Routed Design Report
Scrambler ASIC IP Core

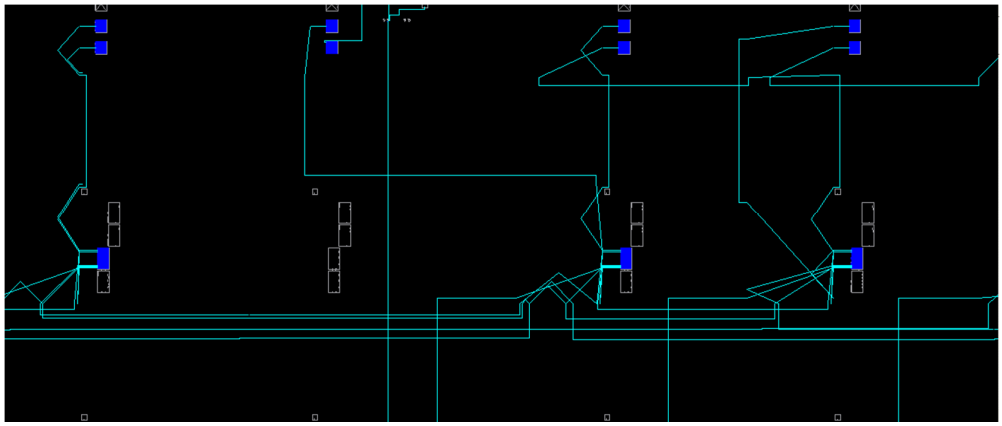

Figure 12. Scrambler ASIC Routed Design

DESIGN FLOW REPORT-DE-SCRAMBLER ASIC IP CORE

RTL Block – De-Scrambler ASIC IP Core

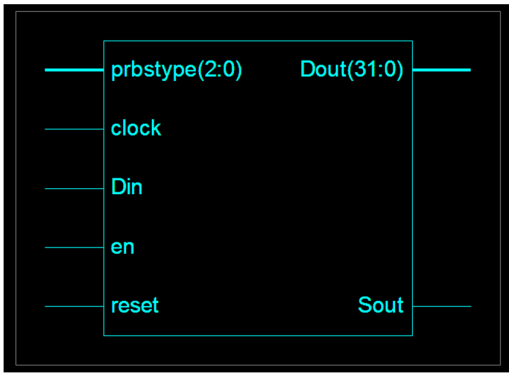

Figure 13. De-Scrambler ASIC RTL Block

RTL Schematic

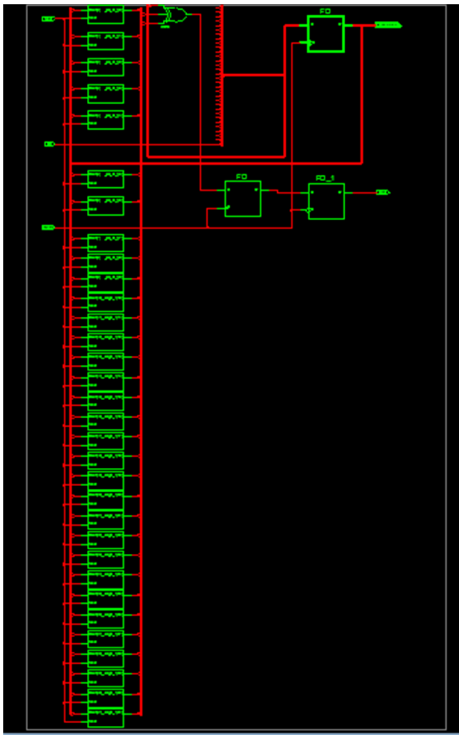

Figure 14. De-Scrambler ASIC Schematic

FPGA Placed Design Report

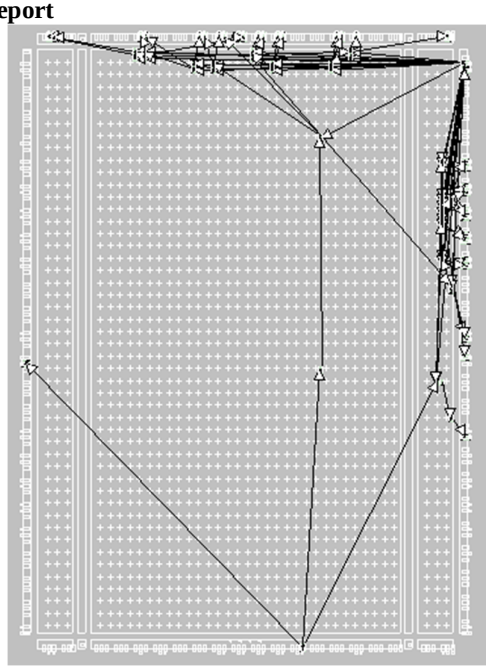

Figure 15. De-Scrambler ASIC Placed Design

FPGA Routed Design Report

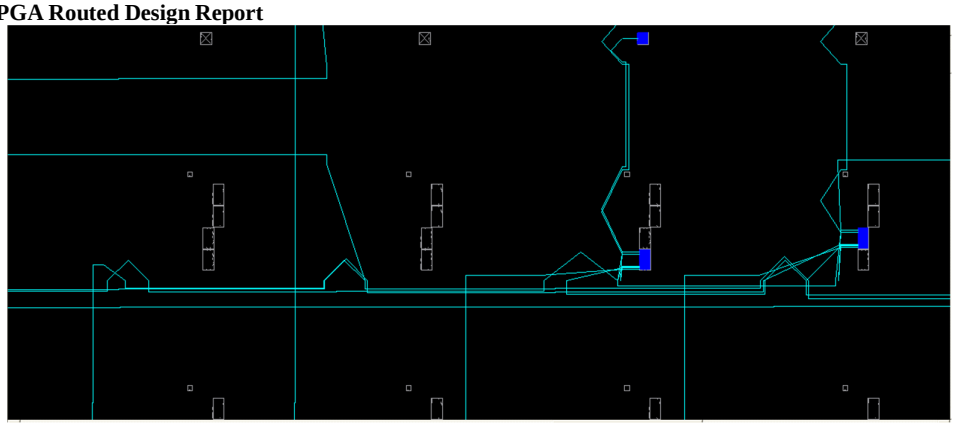

Figure 16. De-Scrambler ASIC Routed Design

ACKNOWLEDGEMENTS

We discussed and cooperated with each other lot for generation of the design. I am very thankful to my supervisor Dr.S.Vathsal, and also to Dr.D.N.Rao in all aspects.

CONCLUSION

This design is very suit for Data Accuracy and Speed of High Speed wireless Application Products like WIFI, Internet, and Cloud etc The main intention of designing scrambler and De-Scrambler is for reduction of noise for getting accurate signal data by data encryption and decryption of different PRBS Pattern Sequences.

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